WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a first memory array having a plurality of first memory cells provided at points where a first data line group including a first data line, a second data line, a third data line, and a fourth data line intersect a plurality of first word lines;

a second memory array having a plurality of second memory cells provided at points where a second data line group including a fifth data line, a sixth data line, a seventh data line, and an eighth data line intersect a plurality of second word lines; and

a first sense amplifier block provided between the first memory array and the second memory array and including a first sense amplifier and a second sense amplifier adjacent to each other;

wherein the first sense amplifier is connected to the first data line and one data line of the second data line group so as to take an open data line arrangement,

the second sense amplifier is connected to the fourth data line and another data line of the second data line group so as to take an open data line arrangement, and

the second and third data lines are placed between the first data line and the fourth data line.

2. The semiconductor device according to claim 1, wherein

one data line of the second data line group connected to the first sense amplifier is the sixth data line,

another data line of the second data line group connected to the second sense amplifier is the seventh data line, and

the sixth and seventh data lines are placed between the fifth data line and the eighth data line.

3. The semiconductor device according to claim 1, wherein the first sense amplifier block further includes a ninth data line and a tenth data line both connected to the first sense amplifier, and includes an eleventh data line and a twelfth data line both connected to the second sense amplifier,

the tenth and eleventh data lines are placed between the ninth data line and the twelfth data line,

the first sense amplifier is connected to the first data line through the ninth data line and connected to the sixth data line through the tenth data line, and

the second sense amplifier is connected to the fourth data line through the eleventh data line and connected to the seventh data line through the twelfth data line.

4. The semiconductor device according to claim 3, wherein the first to twelfth data lines are formed in a first wiring layer, and

the first sense amplifier block further includes a contact pad placed between the tenth data line and the eleventh data line

and formed in the first wiring layer.

5. The semiconductor device according to claim 3, wherein the first to twelfth data lines are formed in a first wiring layer, and

the first sense amplifier block further includes a first contact pad placed between the tenth data line and the eleventh data line and formed in the first wiring layer, and includes a second contact pad placed to the opposite side of the eleventh data line with respect to the twelfth data line and formed in the first wiring layer.

6. The semiconductor device according to claim 2, wherein the first sense amplifier block further includes a ninth data line and a tenth data line both connected to the first sense amplifier, and includes an eleventh data line and a twelfth data line both connected to the second sense amplifier,

the tenth and eleventh data line are placed between the ninth data line and the twelfth data line,

the first sense amplifier is connected to the first data line through the ninth data line and connected to the sixth data line through the tenth data line, and

the second sense amplifier is connected to the seventh data line through the eleventh data line and connected to the fourth data line through the twelfth data line.

7. The semiconductor device according to claim 6, wherein

the first to twelfth data lines are formed in a first wiring layer, and

the first sense amplifier block further includes a first contact pad placed between the ninth data line and the tenth data line and formed in the first wiring layer, and includes a second contact pad placed between the eleventh data line and the twelfth data line and formed in the first wiring layer.

8. The semiconductor device according to claim 2, further comprising:

a second sense amplifier block provided at a position to interpose the first memory array with respect to the first sense amplifier block and having a third sense amplifier and a fourth sense amplifier adjacent to each other; and

a third sense amplifier block provided at a position to interpose the second memory array with respect to the first sense amplifier block and having a fifth sense amplifier and a sixth sense amplifier adjacent to each other, and

wherein the third sense amplifier is connected to the second data line, the fourth sense amplifier is connected to the third data line, the fifth sense amplifier is connected to the fifth data line, and the sixth sense amplifier is connected to the eighth data line.

9. The semiconductor device according to claim 1, wherein one data line of the second data line group connected to the first

sense amplifier is the fifth data line,

another data line of the second data line group connected to the second sense amplifier is the eighth data line, and

the sixth and seventh data lines are placed between the fifth data line and the eighth data line.

10. The semiconductor device according to claim 9, wherein the first sense amplifier block further includes a ninth data line and a tenth data line connected to the first sense amplifier, and includes an eleventh data line and a twelfth data line connected to the first sense amplifier,

the tenth and eleventh data line are placed between the ninth data line and the twelfth data line,

the first sense amplifier is connected to the first data line through the ninth data line and connected to the fifth data line through the tenth data line, and

the second sense amplifier is connected to the eighth data line through the eleventh data line and connected to the fourth data line through the twelfth data line.

11. The semiconductor device according to claim 10, wherein the first to twelfth data lines are formed in a first wiring layer, and

the first sense amplifier block includes a first contact pad placed between the ninth data line and the tenth data line and formed in the first wiring layer, and includes a second contact

pad placed between the eleventh data line and the twelfth data line and formed in the first wiring layer.

12. The semiconductor device according to claim 1, wherein the first and fifth data line are aligned on a first virtual line,

the second and sixth data line are aligned on a second virtual line,

the third and seventh data line are aligned on a third virtual line,

the fourth and eighth data line are aligned on a fourth virtual line, and

the first through fourth virtual line are placed in parallel at predetermined interval.

13. The semiconductor device according to claim 1, wherein the first to fourth data line are respectively arranged at intervals greater than or equal to twice the minimum feature size F, and the fifth to eighth data line are respectively arranged at intervals greater than or equal to twice the minimum feature size F.

14. The semiconductor device according to claim 1, wherein the first and second memory array respectively have one intersecting-point type memory matrix structures,

each of the plurality of first and second memory cells includes a switch MISFET and a capacitor, and

each of the first to fourth sense amplifiers includes P-type

MISFET pairs whose drains and gates are cross-coupled and whos sources are commonly connected, and N-type MISFET pairs whose drains and gates are cross-coupled and whose sources are commonly connected.

15. The semiconductor device according to claim 1, wherein each of the plurality of first and second memory cells includes a switch MISFET and a capacitor and have areas each equal to about six times the square of the minimum feature size F with respect to the minimum feature size F.

16. The semiconductor device according to claim 1, wherein the first through eighth data lines are formed by lithography technique using a phase shift mask.

17. A semiconductor device comprising:

a first memory array including a plurality of first memory cells provided at points where a first data line, a second data line, a third data line, and a fourth data line intersect a plurality of first word lines;

a second memory array including a plurality of second memory cells provided at points where a fifth data line, a sixth data line, a seventh data line, and an eighth data line intersect a plurality of second word lines; and

a first sense amplifier block provided between the first memory array and the second memory array and including a first sense amplifier and a second sense amplifier adjacent to each

other, a ninth data line and a tenth data line both connected to the first sense amplifier, and an eleventh data line and a twelfth data line both connected to the second sense amplifier;

wherein the first sense amplifier is connected to the first data line through the ninth data line and connected to the sixth data line through the tenth data line so as to take an open data line arrangement,

the second sense amplifier is connected to the eighth data line through the eleventh data line and connected to the third data line through the twelfth data line so as to take an open data line arrangement, and

the second data line is placed between the first and third data lines, the third data line is placed between the second and fourth data lines, the sixth data line is placed between the fifth and seventh data lines, the seventh data line is placed between the sixth and eighth data lines, and the tenth and eleventh data lines are placed between the ninth and twelfth data lines.

18. The semiconductor device according to claim 17, wherein the first to twelfth data lines are formed in a first wiring layer, and

the first sense amplifier block is placed between the tenth data line and the eleventh data line and has a contact pad formed in the first wiring layer.

19. The semiconductor device according to claim 17, wherein

the first to twelfth data lines are formed in a first wiring layer, and

the first sense amplifier block includes a first contact pad placed between the tenth data line and the eleventh data line and formed in the first wiring layer, and a second contact pad placed on the opposite side of the eleventh data line with respect to the twelfth data line and formed in the first wiring layer.

20. The semiconductor device according to claim 17, further including a second sense amplifier block provided at a position to interpose the first memory array with respect to the first sense amplifier block and having a third sense amplifier and a fourth sense amplifier adjacent to each other, and

a third sense amplifier block provided at a position to interpose the second memory array with respect to the first sense amplifier block and having a fifth sense amplifier and a sixth sense amplifier adjacent to each other, and

wherein the third sense amplifier is connected to the second data line, the fourth sense amplifier is connected to the fourth data line, the fifth sense amplifier is connected to the fifth data line, and the sixth sense amplifier is connected to the seventh data line.

21. The semiconductor device according to claim 17, wherein each of the plurality of first and second memory cells includes a switch MISFET and a capacitor, and the respective areas of the

plurality of first and second memory cells are about six times the square of the minimum feature size F with respect to the minimum feature size F.

22. The semiconductor device according to claim 17, having a mirror-reflected inverted structure by a mirror reflection axis provided between the first sense amplifier and the second sense amplifier.

23. A semiconductor device comprising:

a first memory array including a plurality of first memory cells provided at points where a first data line, a second data line, a third data line, and a fourth data line intersect a plurality of first word lines;

a second memory array including a plurality of second memory cells provided at points where a fifth data line, a sixth data line, a seventh data line, and an eighth data line intersect a plurality of second word lines; and

a first sense amplifier block provided between the first memory array and the second memory array and including a first sense amplifier and a second sense amplifier adjacent to each other,

wherein the first sense amplifier is connected to the first data line and the sixth data line so as to take an open data line arrangement,

the second sense amplifier is connected to the third data

line and the eighth data line so as to take an open data line arrangement,

the second data line is placed between the first and third data lines, the third data line is placed between the second and fourth data lines, the sixth data line is placed between the fifth and seventh data lines, and the seventh data line is placed between the sixth and eighth data lines, and

the first to fourth data lines are respectively placed at intervals greater than or equal to about three times the minimum feature size F, and the fifth to eighth data lines are respectively placed at intervals greater than or equal to about three times the minimum feature size F.

24. The semiconductor device according to claim 23, wherein the first sense amplifier block further includes a ninth data line and a tenth data line both connected to the first sense amplifier, an eleventh data line and a twelfth data line both connected to the second sense amplifier, a first drive line, and a second drive line,

each of the first and second sense amplifiers includes P-type MISFET pairs formed in an N-type semiconductor region, whose drains and gates are cross-coupled and whose sources are commonly connected, and includes N-type MISFET pairs formed in a P-type semiconductor region, whose drains and gates are cross-coupled and whose sources are commonly connected,

the first through twelfth data lines are formed in a first wiring layer formed above the N-type and P-type semiconductor regions,

the first and second drive lines are formed in a second wiring layer formed above the first wiring layer,

the tenth and eleventh data lines are placed between the ninth data line and the twelfth data line,

the sources of the P-type MISFET pairs of the first and second sense amplifiers are connected to the first drive line via a first through hole provided between the tenth and eleventh data lines, and

the sources of the N-type MISFET pairs of the first and second sense amplifiers are connected to the second drive line via a second through hole provided between the tenth and eleventh data lines.

25. The semiconductor device according to claim 23, wherein a phase shift mask in which a phase assigned to patterns for the first, third, fifth, and seventh data lines and a phase assigned to patterns for the second, fourth, sixth and eighth data lines are different from one another by 180 degrees, are used for forming the first to eighth data lines.

26. The semiconductor device according to claim 23, wherein the minimum feature size F is less than or equal to 0.15μm.

27. A semiconductor device comprising:

a first memory array including a plurality of first memory cells provided at points where a plurality of first data lines intersect a plurality of first word lines;

a second memory array including a plurality of second memory cells provided at points where a plurality of second data lines intersect a plurality of second word lines; and

a sense amplifier block provided in a region between the first memory array and the second memory array and including a first sense amplifier and a second sense amplifier adjacent to each other,

wherein the first sense amplifier is connected to one of the plurality of first data lines and one of the plurality of second data lines so as to take an open data line arrangement,

the second sense amplifier is connected to another one of the plurality of first data lines and another one of the plurality of second data lines so as to take an open data line arrangement, and

the plurality of first and second memory cells respectively have an area ($6F^2$) equal to about six times the square of the minimum feature size F.

28. The semiconductor device according to claim 27, wherein the plurality of first data lines are formed by a phase shift method for providing opening patterns with a phase difference of about 180 degree developed between the adjacent first data

lines, and

the plurality of second data lines are formed by the phase shift method for providing opening patterns with a phase difference of about 180 degree developed between the adjacent second data lines.

29. The semiconductor device according to claim 27, wherein the plurality of first data lines are formed by a phase shift method for providing opening patterns with a phase difference of about 180 degree developed between the adjacent first data lines, and

the plurality of second data lines are formed by phase shift masks, each having opening patterns with a phase difference of about 180 degree developed between the adjacent second data lines.

30. The semiconductor device according to claim 27, wherein one of the plurality of first data lines connected to the first sense amplifier and another one of the plurality of first data lines connected to the second sense amplifier are formed by a phase shift mask, each having opening patterns with a phase difference of about 180 degree developed therebetween, and

one of the plurality of second data lines connected to the first sense amplifier and another one of the plurality of second data lines connected to the second sense amplifier are formed by a phase shift mask, each having opening patterns with a phase difference of about 180 degree developed therebetween.